GF40: 3.3V GPIO

Libraries

Name	Process	Form Factor
RGO_GF40_25V33_LP_20C	LP	Staggered CUP
RGO_GF40_25V33_LP_40C	LP	Inline CUP

Summary

The 3.3V GPIO library provides general purpose bidirectional I/O cells. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

Additionally, this library provides a full complement of cells to support the assembly of a functional pad ring by abutment for GPIO and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

This 40nm library is available in both staggered CUP and inline CUP wire bond implementations with a staggered flip chip option.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 200V ESD Machine Model (MM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

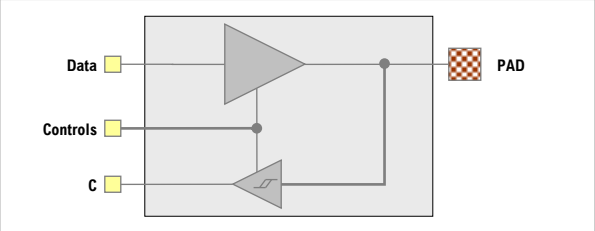
Cell Size & Form Factor

- Staggered (pad-limited) – 20µm x 180µm
- Inline (core-limited) – 44µm x 92µm

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.90	1.0	1.10	V
		0.99	1.1	1.21	V
		1.08	1.2	1.26	V
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.70	3.0	3.30	V
		2.52	2.8	3.08	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	175	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

SRx_BI_SDS_33V_STB



Bidirectional GPIO Driver Features

- Multi-Voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V)
- LVCMOS / LVTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (hi-Z/pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Support Cells

Name	Description
Digital Pads	
STx_IN_001_33V_NC	Input-only buffer
I/O Power / Ground Pads	
PWx_VD_PDO_33V	I/O power (DVDD) with POC
PWx_VD_RDO_33V	I/O power (DVDD)
PWx_VS_RDO_33V	I/O ground (DVSS)
Core Power / Ground Pads	
PWx_VD_RCD_12V	Core power (VDD)
PWx_VS_RCD_12V	Core ground (VSS)
Analog Pads	
ANx_BI_DWR_33V	Isolated analog input cell
Analog Power / Ground Pads	
PWx_VD_ANA_12V	Analog power (AVDD) 1.0V
PWx_VS_ANA_12V	Analog ground (AVSS)
PWx_VD_ANA_33V	Analog power (ADVDD) 3.3V
PWx_VS_ANA_33V	Analog ground (ADVSS)
Support Pads	
SPx_CO_000_33V	Corner cell (rail splitter)
SPx_CO_001_33V	Corner cell (continuous)
SPx_SP_000_33V	0.1µm spacer
SPx_SP_001_33V	1µm spacer
SPx_SP_005_33V	5µm spacer
SPx_SP_010_33V	10µm spacer
SPx_RS_005_33V	Rail splitter

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
1.2	FF	+5%	+10%	-40°C
	FFF	+5%	+10%	125°C
	FFF	+5%	+10%	150°C
	FFF	+5%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C
1.1 / 1.0	FF	+10%	+10%	-40°C
	FFF	+10%	+10%	125°C
	FFF	+10%	+10%	150°C
	FFF	+10%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C

[1] DVDD = 1.8, 2.5, 2.8, 3.0 and 3.3V

CUP Cells

Staggered CUP Cells	
CUP_GF40_70P1X33P4_IN	70.1µm X 33.4µm Inner
CUP_GF40_70P1X33P4_OUT	70.1µm X 33.4µm Outer
CUP_GF40_70P1X48P4_IN	70.1µm X 48.4µm Inner
CUP_GF40_70P1X48P4_OUT	70.1µm X 48.4µm Outer
CUP_GF40_FC	Flip chip structure
CUP_GF40_82P5X59P4_IN	82.5µm X 59.4µm In - Cu bond
CUP_GF40_82P5X59P4_OUT	82.5µm X 59.4µm Out - Cu bond
CUP_GF40_W48P4XL82P5_IN	48.4µm X 82.5µm In - Cu bond
CUP_GF40_W48P4XL82P5_OUT	48.4µm X 82.5µm Out - Cu bond
Inline CUP Cells	
CUP_GF40_INL_84X37P4	84µm X 37.4µm Inline
CUP_GF40_INL_84X50	84µm X 50µm Inline

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